Amendments to the Claims:

1. (Previously Presented) An apparatus comprising:

a memory;

a plurality of functional units that transfer data to and from the memory;

a crossbar that provides a data path from each unit to the memory,

wherein the crossbar comprises an arbitration unit to monitor data traffic generated by each of the plurality of functional units through the crossbar and assigns a priority to each functional unit based on the data traffic, wherein one of the plurality of functional units comprises another crossbar,

wherein the arbitration unit monitors data traffic from each functional unit by monitoring a type of data that each functional unit transfers.

2. (Original) The apparatus defined in claim 1, wherein the arbitration unit monitors data traffic from each functional unit by monitoring how often each functional unit transfers data through the crossbar.

3. (Canceled).

4. (Original) The apparatus defined in claim 1, wherein the arbitration unit uses a programmable priority scheme and a fixed priority scheme.

5. (Original) The apparatus defined in claim 4 wherein the fixed priority scheme comprises a round robin scheme that rotates the top priority designation among at least some of the plurality of units.

6. (Original) The apparatus defined in claim 4 wherein the programmable priority scheme makes changes based on actual traffic statistics.

7. (Original) The apparatus defined in claim 4 wherein the arbitration unit uses a number of rotating slots, each programmed to assign priority to any one of the plurality of functional units.

8. (Original) The apparatus defined in claim 7 wherein the arbitration unit grants access to one functional unit if the one functional unit makes a request while the arbitration unit indicates that the one functional unit is at one of the number of rotating slots having a highest priority.

9. (Previously Presented) An apparatus comprising:

a memory;

a plurality of functional units that transfer data to and from the memory;

a crossbar that provides a data path from each unit to the memory, wherein the crossbar comprises an arbitration unit to monitor data traffic generated by each of the plurality of functional units through the crossbar and assigns a priority to each functional unit based on the data traffic,

wherein the arbitration unit monitors data traffic from each functional unit by monitoring the type of data that each functional unit transfers, wherein the arbitration unit uses a programmable priority scheme and a fixed priority scheme, wherein the arbitration unit uses a number of rotating slots, each programmed to assign priority to any one of the plurality of functional units, wherein the arbitration unit grants access to one functional unit if the one functional unit makes a request while the arbitration unit indicates that the one functional unit is at one of the number of rotating slots having a highest priority, and wherein the arbitration unit only grants access if all necessary resources requested by the one functional unit are available.

10. (Previously Presented) An apparatus comprising:

a memory;

a plurality of functional units that transfer data to and from the memory;

a crossbar that provides a data path from each unit to the memory, wherein the crossbar comprises an arbitration unit to monitor data traffic generated by each of the plurality of functional units through the crossbar and assigns a priority to each functional unit based on the data traffic,

wherein the arbitration unit monitors data traffic from each functional unit by monitoring the type of data that each functional unit transfers, wherein the arbitration unit uses a programmable priority scheme and a fixed priority scheme, wherein the arbitration unit uses a number of rotating slots, each programmed to assign priority to any one of the

plurality of functional units, wherein the arbitration unit grants access to one functional unit if the one functional unit makes a request while the arbitration unit indicates that the one functional unit is at one of the number of rotating slots having a highest priority, and wherein the arbitration unit increments a slot count to change the highest priority to another of the rotating slots after granting access to the one functional unit.

11. (Previously Presented) An apparatus comprising:

a memory;

a plurality of functional units that transfer data to and from the memory;

a crossbar that provides a data path from each unit to the memory, wherein the crossbar comprises an arbitration unit to monitor data traffic generated by each of the plurality of functional units through the crossbar and assigns a priority to each functional unit based on the data traffic,

wherein the arbitration unit monitors data traffic from each functional unit by monitoring the type of data that each functional unit transfers, wherein the arbitration unit uses a programmable priority scheme and a fixed priority scheme, wherein the arbitration unit uses a number of rotating slots, each programmed to assign priority to any one of the plurality of functional units, wherein the arbitration unit grants access to one functional unit if the one functional unit makes a request while the arbitration unit indicates that the one functional unit is at one of the number of rotating slots having a highest priority, and wherein the arbitration unit uses the fixed priority scheme to grant access to one of the plurality of functional units when the one functional unit makes a request, is not assigned to a slot with the highest priority, and a functional unit with the highest priority is not making a request or a desired resource of the functional unit with the highest priority is not available.

12. (Previously Presented) The apparatus defined in claim 1 further comprising:

a central processing unit (CPU); and

an access bus coupled to the CPU and plurality of functional units, the access bus being independent of the data path.

13. (Canceled).

14. (Original) The apparatus defined in claim 1 wherein the arbitration unit further comprises a direct memory access (DMA) port request unit that allows access priorities to the memory to be programmably defined.

15. (Original) The apparatus defined in claim 1 wherein the arbitration unit further comprises statistics registers that indicate usage of the data paths.

16. (Original) The apparatus defined in claim 15 wherein the statistics registers store a count of the number of data transfers through the crossbar.

17. (Original) The apparatus defined in claim 15 wherein the arbitration unit dynamically adjusts the priority assigned to each functional unit based on bandwidth demand requests by each functional unit.

18. (Original) The apparatus defined in claim 15 wherein the arbitration unit dynamically adjusts the priority assigned to each functional unit based on delays in getting requests serviced.

19.-20. (Canceled)